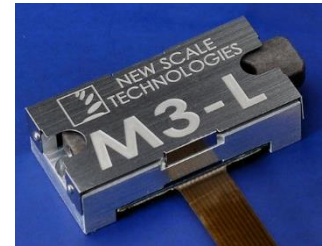


M3-L Linear Actuator SPI /SS Line Always Asserted



The SPI Bus Issue

M3-L modules with the **PIC24FJ64GP202** processor and F/W 4.7.x or earlier, treat the SPI /SS input as always asserted. That means if any other devices are connected to the same SPI bus and the host attempts to select a different device, the M3-L module will still buffer and attempt to process data being sent over the SPI bus. If, for example, two M3-L modules were connected to the same bus, both modules would respond to commands sent by the host even if the host selects only one of the two modules.

However, if you use the I2C bus (or your M3-L has been converted to use the UART bus instead of SPI) this does not affect you.

Why is it Happening

This happens because, by default, the PIC24FJ64GP202 supports a secondary oscillator input whose pin is also the module's SPI /SS (chip select) pin which makes that pin always appear to be asserted.

Getting it Fixed

If you have one or more M3-L modules with the PIC24FJ64GP202 processor (w/ F/W V4.7.x or earlier) and use the SPI bus, you may contact New Scale Technologies to have the M3-L returned for reprogramming so that the secondary oscillator input may be disabled. This issue cannot be corrected with a field firmware update as it requires a change to the processor's configuration registers.

How to Confirm your M3-L has the PIC24FJ64GP202 Processor

If your M3-L reports F/W V4.5.5 or earlier, it does not have the PIC24FJ64GP202 processor. If the M3-L reports F/W V4.6.2 or V4.7.x, you can confirm whether you have the PIC24FJ64GP202 processor by checking the backside of the module where the processor is visible (see the outlined area in the image below).



Appearance of the PIC24FJ64GP202 Processor on Backside of M3-L Module at U1

For More Information

Visit newscaletech.com to contact our tech support team or email NST at nstsales@newscaletech.com.

Revision history

Date	Changes
7.28.2025	Created